

WHAT IS CLAIMED IS:

1. A method of calculating, by the use of a computer, a numerical value  $V_A$  representative of a circuit property of a logic level circuit, from a numerical value  $V_B$ , which shows a block property of a logic block included in the logic level circuit, comprising the steps of:

- (a) calculating the  $V_B$  from numerical values  $V_C$ 's each of which represents a transistor property of a transistor included in the logic block; and,
- (b) calculating the  $V_A$  from the  $V_B$ .

2. A method as in claim 1 wherein, in the step (a), each  $V_C$  shows a specific one of the transistor property of the transistor connected to an input pin of the logic block and another  $V_C$  shows another specific one of the transistor property of the transistor connected to an output pin of the logic block.

3. A method of calculating, by the use of a computer, a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, comprising the steps of:

- (a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect;
- (b) calculating variations of delay times that signals pass through transistors connected to the input and output pin caused by said aging; and,
- (c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b).

4. A method of calculating, by the use of a computer, pin-to-pin delay time  $T_{\text{io path\_aged}}$ , which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time  $T_{\text{connect\_aged}}$ ,

which is delay time of a signal passing between said two logic blocks connected to each other, comprising the steps of:

(a) calculating an amount of stress  $S_{in}$  cast by the input pin and an amount of stress  $S_{out}$  cast by the output pin according to the following expression:

when it is assumed that a load capacitance is represented by  $C$  [pF], constants

$$S = \alpha \left( \frac{C}{W} \right)^\beta$$

depending on change of inputted waveform are represented by  $\alpha$  and  $\beta$ , and width of channel of the transistor connected to the pin is represented by  $W$  [ $\mu m$ ];

(b) calculating an aged delay time of the input pin  $\delta_{in}$  [%] and an aged delay time  $\delta_{out}$  [%] according to the following expression:

when it is assumed that a constant depending on physical structure of the pin

$$\delta = \gamma \left( \frac{\tau S f}{\epsilon_1 e^{\kappa T}} \right)^{\frac{1}{\epsilon_2}}$$

is represented by  $\gamma$ , the term of a guarantee of the LSI is represented by  $\tau$  [hour], constants depending on process are represented by  $\epsilon_1$ ,  $\epsilon_2$  and  $\kappa$ , working frequency is represented by  $f$  [Hz], and absolute temperature is represented by  $T$  [K];

(c) calculating the pin-to-pin delay time  $T_{iopath\_aged}$  and the block-to-block delay time  $T_{connect\_aged}$  according to the following expressions:

when it is assumed that pin-to-pin delay time and block-to-block delay time

$$T_{iopath\_aged} = T_{iopath\_fresh} (1 + \lambda_{in} \delta_{in} + \lambda_{out} \delta_{out})$$

$$T_{connect\_aged} = T_{connect\_fresh} (1 + \lambda_{out} \delta_{out})$$

calculated ignoring aging caused by hot carrier effect are represented by

$T_{\text{io path\_fresh}}$  [ps] and  $T_{\text{connected\_fresh}}$  [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by  $\lambda_{\text{in}}$  and  $\lambda_{\text{out}}$ .

5. A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising the steps of:

(a) calculating delay times of all said logic blocks according to the method as in claim 3; and,

(b) calculating the delay time of the logic level circuit from the result of step (a).

6. A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising the steps of:

(a) calculating delay times of all said logic blocks according to the method as in claim 4; and,

(b) calculating the delay time of the logic level circuit from the result of step (a).

7. A computer software product for calculating a numerical value  $V_A$ , which shows a property of a logic level circuit, from a numerical value  $V_B$ , which shows a property of a logic block constituting the logic level circuit, the product making a computer execute the following processes:

(a) calculating the  $V_B$  from numerical value  $V_C$ 's each of which shows property of a transistor constituting part of the logic block; and,

(b) calculating the  $V_A$  from the  $V_B$ .

8. A computer software product as in claim 7 wherein in process (a) one  $V_C$  shows a property of a transistor connected to an input pin of the logic block and another  $V_C$  shows a property of a transistor connected to an output pin of the logic block.

9. A computer software product for calculating a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the product making a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect;

(b) calculating variations of delay times that signals pass through transistors connected to the input and output pin caused by said aging; and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b).

10. A computer software product for calculating pin-to-pin delay time  $T_{iopath\_aged}$ , which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time  $T_{connect\_aged}$ , which is delay time of a signal passing between said two logic blocks connected to each other by a computer, the product making a computer execute the following processes:

(a) calculating an amount of stress  $S_{in}$  cast by the input pin and an amount of stress  $S_{out}$  cast by the output pin according to the following expression:

when it is assumed that a load capacitance is represented by  $C$  [pF], constants

$$S = \alpha \left( \frac{C}{W} \right)^\beta$$

depending on change of inputted waveform are represented by  $\alpha$  and  $\beta$ , and width of channel of the transistor connected to the pin is represented by  $W$  [ $\mu m$ ];

(b) calculating an aged delay time of the input pin  $\delta$  in [%] and an aged delay time  $\delta$  out [%] according to the following expression: when it is assumed that a constant depending on physical structure of the pin

$$\delta = \gamma \left( \frac{\tau S f}{\varepsilon_1 e^{\kappa T}} \right)^{\frac{1}{\varepsilon_2}}$$

is represented by  $\gamma$ , the term of a guarantee of the LSI is represented by  $\tau$  [hour], constants depending on process are represented by  $\varepsilon_1$ ,  $\varepsilon_2$  and  $\kappa$ , working frequency is represented by  $f$  [Hz], and absolute temperature is represented by  $T$  [K];

(c) calculating the pin-to-pin delay time  $T_{iopath\_aged}$  and the block-to-block delay time  $T_{connect\_aged}$  according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh} (1 + \lambda_{in} \delta_{in} + \lambda_{out} \delta_{out})$$

$$T_{connect\_aged} = T_{connect\_fresh} (1 + \lambda_{out} \delta_{out})$$

when it is assumed that pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by  $T_{iopath\_fresh}$  [ps] and  $T_{connect\_fresh}$  [ps], and ratios of delay times occurred at the input stage and the output stage to whole delay time occurred from the input pin to the output pin are represented by  $\lambda_{in}$  and  $\lambda_{out}$ .

11. A computer software product for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the product making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the product as in claim 9; and,

(b) calculating the delay time of the logic level circuit from the result of step (a).

